REMARKS

Claims 1-9 and 34-42 are all the claims pending in the application. Claims 3-4 and 7-8 have been allowed. Claims 1-2, 5-6, 9 and 34-42 stand rejected on prior art grounds. Applicants respectfully traverse these objections/rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1, 2, 6, 9 and 36 stand rejected under 35 U.S.C. §102(b) as being anticipated by Wu, et al., hereinafter "Wu" (6,770,516). Claims 34-35 and 37-40 stand rejected under 35 U.S.C. §103(a) as being anticipated by Wu, in view of Lin, et al., hereinafter "Lin" (6,800,910). Claims 41-42 stand rejected under 35 U.S.C. §103(a) as being anticipated by Wu, in view of Lin, and in further view of Yuzurihara, et al., hereinafter "Yuzurihara" (5,218,232). Applicants respectfully traverse these rejections based on the following discussion.

A. The Rejection Based on Wu

Applicants respectfully traverse this rejection because Wu does not teach or suggest separate FinFET transistors that are separated by insulating fin that "has approximately the same width dimensions as said first fin and said second fin, such that the spacing between said first FinFET and said second FinFET is approximately equal to the width of one fin" as defined by independent claims 1 and 6. Wu discloses a process whereby fins are etched from a laminate structure (Figure 2) and are eventually separated by an insulator 8 (Figure 11B). Wu does not disclose an insulating fin such as Applicants' claimed fin 104 (Figure 1) much less an insulating fin that has approximately the same width dimensions as the adjacent fins. Therefore, it is Applicants position that Wu does not anticipate independent claims 1 or 6.

The inventive process produces a structure that almost doubles the density of FinFET devices. One advantage of using spacer technology is that spacers can have sizes that are smaller

than the minimum-sized lithographic feature that can be formed using state of the art lithographic techniques. The invention utilizes spacer technology to form the fins, which allows the fins of different transistors to be formed much closer together (only separated by one spacer width) and allows the fins to be sub-lithographic in size. In addition, the spacers are self aligned with the mesa structure and each other, which eliminates the need to align the spacers. The invention also provides a method to form pairs of fins, which could be formed into transistors, or used as wires or resistors to contact each fin independently.

Thus, as shown above, Wu does not teach or suggest "said insulator fin has approximately the same width dimensions as said first fin and said second fin, such that the spacing between said first FinFET and said second FinFET is approximately equal to the width of one fin" (independent claims 1 and 6) and independent claims 1 and 6 are not anticipated by Wu. Further, dependent claims 2, 6, 9, and 36 are similarly patentable, not only by virtue of their dependency from a non-anticipated independent claim, but also because of the additional features of the invention they define. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

B. The Rejection Based on Wu and Lin

Applicants respectfully traverse this rejection because neither Wu nor Lin teach or suggest separate FinFET transistors that are separated by insulating fin that "has approximately the same width dimensions as said first fin and said second fin, such that the spacing between said first FinFET and said second FinFET is approximately equal to the width of one fin" as defined by independent claims 1, 6, and 37.

As shown above, Wu discloses a process whereby fins are etched from a laminate structure (Figure 2) and are eventually separated by an insulator 8 (Figure 11B). Wu does not disclose an insulating fin such as Applicants' claimed fin 104 (Figure 1) much less an insulating fin that has approximately the same width dimensions as the adjacent fins. Therefore, it is Applicants position that Wu does not teach or suggest the structure independent claims 1, 6 or 10/604,206

37.

Similarly, Lin discloses a process whereby a fin is etched (Figure 5c) and eventually covered by an insulator (not shown). Lin does not disclose an insulating fin such as Applicants' claimed fin 104 (Figure 1) much less an insulating fin that has approximately the same width dimensions as the adjacent fins. Therefore, it is Applicants position that Lin does not teach or suggest the structure independent claims 1, 6 or 37. Therefore, no combination of Wu or Lin would teach or suggest the invention defined by independent claims 1, 6, and 37, and such claims are patentable over the prior art of record.

As mentioned above, the inventive process produces a structure that almost doubles the density of FinFET devices. One advantage of using spacer technology is that spacers can have sizes that are smaller than the minimum-sized lithographic feature that can be formed using state of the art lithographic techniques. The invention utilizes spacer technology to form the fins, which allows the fins of different transistors to be formed much closer together (only separated by one spacer width) and allows the fins to be sub-lithographic in size. In addition, the spacers are self aligned with the mesa structure and each other, which eliminates the need to align the spacers. The invention also provides a method to form pairs of fins, which could be formed into transistors, or used as wires or resistors to contact each fin independently.

Thus, as shown above, the proposed combination of Wu and Lin does not teach or suggest "said insulator fin has approximately the same width dimensions as said first fin and said second fin, such that the spacing between said first FinFET and said second FinFET is approximately equal to the width of one fin" (independent claims 1, 6, and 37) and independent claims 1, 6, and 37 are patentable over the proposed combination of Wu and Lin. Further, dependent claims 34, 35, and 37-40 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also because of the additional features of the invention they define. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

C. The Rejection Based on Wu, Lin, and Yuzurihara

Yuzurihara is referenced for the limited purpose of the gate having a first impurity doping region and a second impurity doping region to allow the gate to have different work functions. Yuzurihara is not supplied to teach (and does not teach or suggest) and insulator fin that "has approximately the same width dimensions as said first fin and said second fin, such that the spacing between said first FinFET and said second FinFET is approximately equal to the width of one fin." Yuzurihara does not utilize fins and does not create FinFET's. Therefore, Yuzurihara cannot teach or suggest the claimed insulating fin that permits closely spaced, yet insulated separate FinFET's as in the claimed invention. As shown above, neither Wu nor Lin teach or suggest this feature and, therefore, no combination of Wu, Lin, and Yuzurihara would teach or suggest this feature. Therefore, it is Applicants position that the proposed combination of Wu, Lin, and Yuzurihara does not teach or suggest the inventive insulator fin defined by independent claim 37.

Thus, as shown above, the proposed combination of Wu, Lin, and Yuzurihara does not teach or suggest "said insulator fin has approximately the same width dimensions as said first fin and said second fin, such that the spacing between said first FinFET and said second FinFET is approximately equal to the width of one fin" (independent claim 37) and independent claim 37 is patentable over the proposed combination of Wu, Lin, and Yuzurihara. Further, dependent claims 41-42 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also because of the additional features of the invention they define. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

III. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 1-9 and 34-42, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in 10/604,206

condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

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